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Description

METHOD AND STRUCTURE OF VERTICAL STRAINED SILICON DEVICES

BACKGROUND OF INVENTION

[0001] The field of the invention is that of integrated circuit processing, in particular DRAM cells having vertical pass transistors.

[0002] In the fabrication of vertical-transistor DRAM cells, both in DRAMs and in DRAM arrays in ASICs and other complex systems, the formation of the capacitor removes silicon from the trench walls in the upper part of the trench, producing an overhang of the pad nitride.

[0003] That overhang interferes with filling the upper part of the trench with the gate electrode, leaving voids in the gate electrode that are disadvantageous.

[0004] Further, for a given ground rule and inter-cell spacing, the space for bitline contacts to the upper electrode of the vertical transistor is limited. The removal of silicon from the upper trench walls further reduces the width of the

bitline contacts, extending outward from the trench walls into the silicon well.

[0005] Expanding the width of the cell to accommodate a wider trench and a wider bitline contact is not an option, given the overwhelming need to reduce the transverse dimensions of the cells.

[0006] As the demand for higher performance devices increases steadily, one attractive option is the use of strained silicon to improve electron mobility.

SUMMARY OF INVENTION

[0007] A feature of the invention is compensation for the overhang of the pad nitride in a trench capacitor vertical-transistor DRAM cell by forming an epitaxial strained silicon layer on the trench walls that improves transistor mobility.

[0008] Another feature of the invention is that the added silicon removes voids from the poly trench fill.

[0009] Yet another feature of the invention is that the extra width of the added silicon reduces resistance on the bitline contact.

[0010] Yet another feature of the invention is that forming a vertical strained silicon channel improves the performance of the vertical device.

Brief Description of Drawings

[0011] Figure 1 illustrates a sample wafer after an initial step of etching a deep trench.

[0012] Figure 2 illustrates the same area after forming the cell capacitor and the collar oxide.

[0013] Figure 3 illustrates the cell after forming the aperture for the buried strap.

[0014] Figure 4 illustrates the cell after forming the buried strap.

[0015] Figure 5 illustrates the cell after forming the trench top oxide.

[0016] Figure 6 illustrates the cell after the epi step.

[0017] Figure 7 illustrates the cell after growing the gate oxide and filling the gate electrode.

[0018] Figure 8 illustrates the cell after forming the array top oxide.

[0019] Figure 9 illustrates the cell after forming gate contacts.

[0020] Figure 10A and Figure 10B illustrate the cell after forming bitline contacts.

Detailed Description

[0021] Figure 1 shows a wafer for use in the invention, in which substrate 10 is a bulk silicon substrate, on which is

formed a buffer layer 20 of SiGe alloy and a device layer 30, also of SiGe. A layer of strained silicon will be formed on the vertical face of the layer of SiGe. A transistor body will be formed within this vertical layer of strained silicon. Pad oxide 42 and pad nitride 45 complete the structure.

[0022] Layer 20 is formed on the surface of substrate 10 to accommodate the difference in atomic spacing of the two materials. There will be dislocations and other material defects in layer 20 that would be detrimental to transistor operation. As is known in the art, layer 30, a fully relaxed SiGe layer, is formed to hold the transistors, not only in the cell illustrated, but also, optionally, in logic circuits containing planar transistors that are formed elsewhere in an integrated circuit that contains the DRAM cell illustrated.

[0023] Aperture 110 is a deep trench, e.g. 8 microns deep, that will contain a DRAM cell having a vertical field effect transistor (FET) for an access device, as is known in the art.

[0024] The invention may be used with a DRAM integrated circuit, or with a circuit having other functions that contains a DRAM array. In contemporary practice, many composite systems that are fabricated in integrated circuit form, include memories that are formed from DRAMs.

[0025] Figure 2 illustrates the same area after some intermediate steps that form a capacitor 100. Capacitor 100 has a dielectric 12, e.g. oxide (SiO2) or a layer of oxide adjacent to a layer of nitride (Si3N4). A central electrode 105, formed by deposition of doped polysilicon (poly) or other conducting materials such as metals, completes the capacitor and will make contact with an access transistor to be constructed in the upper part of the trench.

[0026] A collar 107 (illustratively oxide) has been formed after the completion of the initial portion of the capacitor and before the extension of the central electrode. Oxide collars are conventional and are formed by oxidizing the vertical silicon (and/or the SiGe) exposed by the construction of the trench. Alternatively, the collar may be formed on the trench sidewall by conventional deposition techniques such as chemical vapor deposition (CVD). The deposited material is removed from the trench bottom by techniques such as reactive ion etching (RIE), leaving the collar material on the trench sidewall. Other insulating materials may also be used to form the collar.

[0027] After the collar has been formed, the central portion of the trench is filled with a conducting material such as polysilicon, or a combination of several conducting mate-

rials such as polysilicon and titanium nitride, that is then recessed to leave a portion of the collar exposed.

[0028] In this case, the collar extends below and above the defect-laden layer 20, thus also protecting the other parts of the structure from being affected by defects in layer 20.

[0029] An aperture 111 now remains above the top surface of poly electrode 107. The width of aperture 111 in this Figure, denoted by bracket 112, will be referred to as the original trench width. As can be seen in Figure 2, the process of forming the capacitor and the collar has consumed some of the SiGe in the device layer 30, leaving an overhang below the pad oxide 42 that is denoted by bracket 122. This overhang has presented a problem in the prior art because conventional deposition of materials such as the gate electrode will not completely fill the trench due to the overhang, so that voids tend to form in the filling material.

[0030] Figure 3 shows the same cell after a step of etching the top and inner corners of collar 107 in a wet etch step to form apertures 113 extending transversely from and below the top surface of poly 105.

[0031] Figure 4 shows the result of filling apertures 113 in the poly and then recessing the fill material to leave the new

poly only in the apertures 113, forming buried straps 106.

[0032] Figure 5 shows the result of depositing a layer of insulator 132, referred to as the trench top oxide that fills the space above the central electrode of the capacitor and isolates it from the gate electrode of the vertical transistor that will be deposited.

[0033] At any convenient time, an annealing step drives dopant from the poly 105 and/or from the deposited buried strap into the SiGe device layer to form an extended buried strap 106' that extends the dopant into the device layer, making contact with an area that will be part of the lower electrode of a vertical FET.

[0034] The process of depositing oxide in the aperture and etching any material that has adhered to the trench walls will increase the extent of overhang 122.

[0035] Figure 6 shows the result of an epitaxial deposition of silicon 134, referred to as a body layer, which has been deposited epitaxially on the exposed surface of layer 30. Layer 134 will become part of the body of the vertical FET.

[0036] Epi layer 134 has been deposited to a nominal thickness equal to the length of overhang 122, so that the new vertical surface of the transistor body is substantially aligned with the original trench width defined by the vertical face

of pad nitride 45.

[0037] Since the inter-atomic distance in SiGe is greater than the corresponding distance in crystalline silicon, the silicon in layer 134 is strained. That strain increases the mobility of the vertical transistor and therefore increases the performance of the transistor.

[0038] The transverse dimension of the trench is decreased by twice the thickness of layer 134. The performance of a transistor in a strained silicon layer is greater than the performance of a comparable transistor in a SiGe layer. In some cases, the extra performance may not be required and it may be preferable to put down a layer of SiGe on the vertical face of the SiGe layer and to use that layer as the body of the vertical transistor.

[0039] The transverse dimension of the trench is decreased by twice the thickness of layer 134. For a given ground rule, the dimension of the trench and the spacing between the gate electrode and the passing wordline (shown in Figure 9) is fixed, so that decreasing the trench width frees up area for other purposes, as will be described below.

[0040] Figure 7 shows the result of forming gate dielectric, e.g., thermally grown oxide, on layer 134, filling the remaining aperture with conducting material 154 and then optionally

etching the outer portion of the top of the conducting material 155 to form apertures 156. The conducting material 154 is preferred to be polysilicon.

[0041] Figure 8 shows the result of stripping pad nitride 45, implanting dopant in the upper portion of layer 30 to form, depending on the operation of the transistor, a drain or source 157 of the transistor and filling apertures 156 with array top insulating material 162 such as oxide 162, separating the gate contact 155 from the drain 157. Isolation trenches (not shown) may be formed at any convenient time to isolate cells and devices in the other portion of the circuit.

[0042] The cell is not complete until a contact has been formed to the bitline of the DRAM array (at the upper electrode of the vertical transistor) and a gate contact has been formed to the wordline of the DRAM array (at the gate of the access transistor).

[0043] Figure 9 shows the result of an intermediate step of forming a wordline structure 175 or 177, comprising an extension 172 of the gate contact 155 and associated cap and spacer layers. Polysilicon, tungsten, tungsten silicide, or any other suitable conducting materials, or any of their combination may be used to form the wordline structure.

Layer 172 that is in contact with poly 155 may be capped by an insulating material 176, such as nitride.

[0044] The wordline structures are formed by deposition of a layer 172 of wordline material and a nitride cap. Gate contact lithography defines a stack of conductive member 172 capped with nitride 176.

[0045] Sidewalls 174 are formed on the sides of the gate stack by depositing a nitride layer or other suitable materials by a conventional process such as CVD and etching the flat portions in a directional etching process such as RIE.

[0046] Three structures are shown in Figure 9 - the wordline structure in the center, denoted by numeral 175 and two passing wordline structures 177 that are wordlines for rows of cells in front of and behind the cell illustrated, using a conventional folded wordline layout. Alternatively (not shown), the wordline may be offset from the center of element 155.

[0047] The spacing 182 between the gate contact for the illustrated cell and the passing wordline on the right is set by the groundrules. For a given groundrule, therefore, the increase in trench width caused by the consumption of silicon reduced the space available for the bitline contact for the trench, which has to be outside the trench and not

contacting the passing wordline 177.

[0048] Figure 10A shows the cell after depositing a first layer of interlevel dielectric 182 (BPSG in this case), opening a contact aperture for the bitline contact and filling the aperture with conducting materials such as W or polysilicon to form contact 185.

[0049] The region of the top of the cell denoted with bracket 190 is enlarged in Figure 10B, showing section of array top dielectric 162 penetrated by gate electrode contact 155 in the center and two bitline contacts 185 on the left and right of gate contact 155.

[0050] Above the right bitline contact 185 a bracket labeled 185 indicates the width of the bitline contact according to the invention. Arrow 186 indicates the width in a prior art arrangement in which the layer 134 of strained silicon is not deposited, so that the distance 186 is the width available for the bitline contact – extending from the recessed trench wall on the right to the left edge of arrow 185, which is at the location of the vertical edge of pad nitride 45.

[0051] In the past, the distance between the trench walls as they were recessed into the layer 30 set the width of the trench and therefore by subtraction the width available for the

bitline contact.

[0052] In a cell according to the invention, the added width of the strained silicon 134 narrows the trench aperture and therefore increases the space available for the bitline contact. With a wider contact, the resistance of the electron path in and out of the capacitor is reduced.

[0053] The bottom of bitline contact 185 is in electrical contact with the top of layer 134 and with drain or source 157.

[0054] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.